## ABSTRACT

The PLD that can change the number of input lines and the number of rail between the memories for logic according to the objective logic function, and to which the optimum design can be done to make the size of memory minimum. The memories for logic (4) are arranged in series, and LUT is memorized in them. The input variables are input from the external input lines to each memories for logic (4). The interconnection circuit (5) connects the output lines or the external input lines of memory for logic (4) in the preceding stage and the input lines of memory for logic (4) of the succeeding stage between two memories for logic (4), according to the information for connection memorized in memory for interconnections (6). By rewriting the information for connection according to the objective logic function, the interconnection circuit can be reconfigured, and the number of input lines and the number of rail can be changed. The size of memory can be suppressed to the minimum by optimizing the ratio of the number of rail and the number of input lines according to the logic function.